THIS APPLICATION IS BASED ON THE PROVISIONAL APPLICATION NO. 60/431,977 FILED ON 12/10/2002 AND APPLICATION NO. 10/729,674 FILED ON 12/05/2003

TITLE: A TUNABLE MULTI-BAND RECEIVER BY ON-CHIP SELECTABLE FILTERING

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FRONT PAGE VIEW: FIG. 3

REFEENCES:

[1] U.S. Patent 6,064,866, May 16, 2000, Lange.
[2] U.S. Patent 4,972,509, Nov. 20, 1990, Maejima.

BACKGROUND - TECHNICAL FIELD OF INVENTION

The present invention relates to radio receivers and methods for the reception of RF (radio frequency) communications signals in multiple

frequency bands. In particular, it relates to integrated circuit based radio receivers using programmable on-chip tuning.

BACKGROUND OF THE INVENTION AND DISCUSSION OF PRIOR ART

At the present time, the vast majority of RF communications receivers are of the superheterodyne type. This type of receiver uses one or more IF (intermediate frequency) stages for filtering and amplifying signals at a fixed frequency within an IF chain. This radio architecture has the advantage that fixed filters may be used in the LO chain. In order for the receiver to be useable over multiple bands, its typical architecture is as the dual-band receiver shown in FIG. 1. An RF signal arriving at an antenna 11 passes through a band-select RF filter for each band 13 and 14, an LNA (low noise amplifier) for each band, 15 and 16, and into an image filter for each band, 17 and 18, which produce a band-limited RF signal. This band-limited RF signal then enters a first mixer for each band 19 and 20, which translates the RF signal down to an intermediate frequency by mixing it with the signal produced by the first LOs (local oscillators) 21 and 22. The undesired mixer products in the IF signal are rejected by an IF filter for each band, 23 and 24. The filtered IF signal then enters an IF amplifier stage for each band, 25 and 26, after which the outputs are merged into the second mixer 27 which translates it down to yet another intermediate frequency by mixing it with the signal produced by a second LO, 28. The signal is then sent to the baseband processing. Tuning into a particular channel within the

band-limited RF signal is accomplished by varying the frequency of each LO, 21 and 22.

In order to reduce size, power consumption, and cost, it would be advantageous to integrate the electronic components of radio receivers and reduce the number of filters and mixers. The superheterodyne design, however, requires high quality, narrowband IF bandpass filters that are typically implemented off-chip. These filtering components impose a lower limit to the size, materials cost, assembly cost, and power consumption of receivers built using the superheterodyne design. Moreover, the necessity for mixer and local oscillator circuits operating at high frequencies contributes greatly to the power consumption and general complexity of the superheterodyne receiver. In particular, the high-frequency analog mixers require a large amount of power to maintain linear operation. Although many variations of the superheterodyne design exist, they all share the limitations of the particular design just described.

The growing demand for portable communications has motivated attempts to design radio receivers that permit the integration of more components onto a single chip. Recent advances in semiconductor processing of inductors are allowing more and more of these filters to be implemented on-chip.

A second receiver design is the direct-conversion, or zero-IF, receiver shown in FIG. 2. An antenna 57 couples a RF signal through a first bandpass RF filter for each frequency band, 59 and 60, into a LNA for each frequency band, 61 and 62. The signal then proceeds through a second RF filter 63 and 64, yielding a band-limited RF signal, which then enters a mixer for each frequency band, 65 and 66, and mixes with an LO frequency produced by an LO for each frequency band, 67 and 68. Up to this point, the direct-conversion receiver design is essentially the same as the previous receiver design.

Unlike the previous designs, however, the LO frequency is set to the carrier frequency of the RF channel of interest. The resulting mixer product is a zero-frequency IF signal—a modulated signal at baseband frequency. The mixer outputs, 67 and 68, are combined before being coupled into a lowpass analog filter 69 before proceeding into baseband information signal for use by the remainder of the communications system. In either case, tuning is accomplished by varying the frequency of LOs, 67 and 68, thereby converting different RF channels to zero-frequency IF signals.

Because the direct-conversion receiver design produces a zero-frequency IF signal, its filter requirements are greatly simplified—no external IF filter components are needed since the zero-IF signal is an audio frequency signal that can be filtered by a low-quality lowpass filter. This allows the receiver to be integrated in a standard silicon

process from mixer 65 onwards, making the direct-conversion receiver design potentially attractive for portable applications.

The direct-conversion design, however, has several problems, some of which are quite serious. As with the other designs described above, the RF and image filters required in the direct-conversion design must be high-quality narrowband filters that must remain off-chip. Moreover, this design requires the use of high-frequency mixer and LO circuits that require large amounts of power. Additionally, radiated power from LOs, 67 and 68, can couple into antenna 57, producing a DC offset at the output of mixers, 65 and 66. This DC offset can be much greater than the desired zero-IF signal, making signal reception difficult. Radiated power from LOs 67 and 68, can also affect other nearby direct-conversion receivers tuned to the same radio frequency. Furthermore, to receive signals transmitted using modulation techniques (such as FM) in which access to both the lower and upper sidebands is required, two mixers and two LOs are required to produce both an in-phase and a quadrature baseband signal. Not only does this increase the power required by the receiver, but also the phase between the two LO signals must be precisely maintained at 90 degrees to prevent demodulation distortion. This can be difficult to accomplish with variations in temperature and other operational parameters.

Other prior art to address the multiple frequency band radios use diode-based switches to select the frequency band of interest in a

filter bank as in U.S. Patents 6,064,866[1] and 4,972,509[2]. However, these implementations require a significant number of inductor and capacitor components, and the process of switching a diode element introduces an equivalent impedance element in the resonant tank, thereby reducing the quality (Q) factor of the resonant circuit, thus reducing the performance of the receiver.

In summary, although the prior art includes various receiver designs for multi-band radios, each one has significant disadvantages including one or more of the following: the necessity for several external circuit components, the consumption of large amounts of power, poor signal reception, poor selectivity, distortion, and limited dynamic range.

OBJECTS AND ADVANTAGES OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a multiple frequency band radio receiver design, which has increased integration and decreased power consumption without the operational problems associated with previous receiver designs. It is a further object of the invention to provide an equivalent performance to the traditional multi-band superheterodyne receiver of FIG. 1.

SUMMARY OF THE INVENTION

The present invention achieves the above objects and advantages by providing a new method for multiple frequency band RF

communications signal reception and a new receiver design that incorporates this method. This method includes a method for tuning the receiver to multiple frequency bands without loss of quality factor. In addition, it provides a mechanism to combine the multiple frequency band signals before the mixer, thus requiring only one signal path at the mixers and IF stages.

DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a dual-band superheterodyne receiver considered as prior art.

FIG. 2 is a block diagram of a direct-conversion receiver considered as prior art.

FIG. 3 is a block diagram of a receiver constructed with the principles of the invention.

FIG. 4 is an example of an implementation of the buffer of FIG. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 3 is a block diagram of a dual-band RF communications receiver constructed in accordance with the principles of the present invention. It includes an antenna 73 for coupling a RF signal into the input of a bandpass RF filter, 75 and 76, for each frequency band. The output of the analog bandpass RF filters, 75 and 76, connects to the input of an LNA, 77 and 78, for each frequency band and whose output couples to the input of an image filter, 79 and 80, for each frequency band. The architecture differs from the tradition receiver at this point. Two buffers, 81 and 82, have outputs that are combined

together. Each LNA, 77 and 78, and buffer, 81 and 82, have power down controls, PD1 and PD2, which enable one frequency band to be selected versus the other frequency band. The method of powering down the circuits enables high isolation that is not achievable in other switchable filters in the prior art U.S. Patents 6,064,866[1] and 4,972,509[2]. The combined output is then fed into the first mixer, 83, mixed with the output of the first local oscillator, 84. The output of the first mixer, 83, is then fed into an IF filter, 85, and an IF amplifier, 86. The output of the IF amplifier, 86, is then fed into the second mixer, 87, where it is mixed with the second local oscillator, 88. The savings in this architecture compared to the prior art of FIG. 1 is that one local oscillator, one mixer, one IF filter, and one IF amplifier can be eliminated at the cost of two buffers. This saves in die area and power, as well as board area if the IF filter is implemented as an off-chip component.

FIG. 4 gives a possible implementation of the buffer stage as an emitter follower. The emitter follower circuit consists of a current source, 100, power down control transistors, 101 and 102, a diode-connected transistor, 103, and current mirroring transistor, 104, and a follower transistor, 105. The PD signal, when high, shuts down the currents in transistor, 104, and 105, thus causing the buffer to shut down and isolate its input, IN, from its output, OUT. The operation of this circuit is well known in the art. Additionally, those skilled in the art will recognize that the choices available in type of buffer can include source followers, as well as non-unity gain amplifiers. Those

skilled in the art will also recognize that the power-down signal in the LNA can also be eliminated very little change in functionality. Additionally, those skilled in the art will recognize that more frequency bands can be added to receiver, and that the addition of more frequency bands is within the scope of this patent. These and other modifications, which are obvious to those skilled in the art, are intended to be included within the scope of the present invention. Accordingly, the scope of the invention should be determined not by the embodiment described, but by the appended claims and their legal equivalents.